Lab 7: More Sequential Circuit Analysis and Design

**Primary Objectives:**

1. Get designing and simulating simple sequential logic circuit using flip-flops.

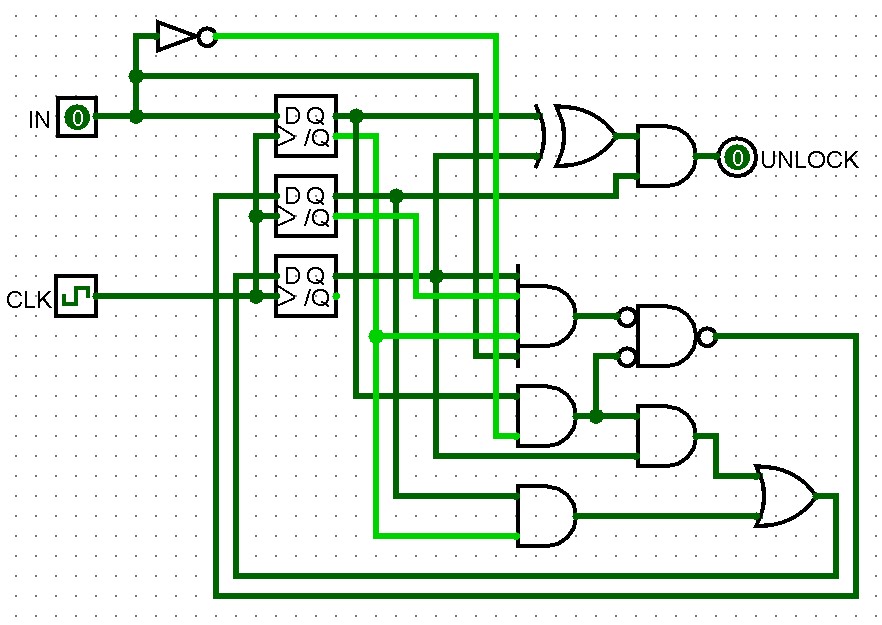
**Sequential Circuit Analysis**

Table 1: Symbol Mapping

|  |  |
| --- | --- |
| Name | Symbol |
| Input | IN |
| Upper D-type flip-flop | Q0 |
| Middle D-type flip-flop | Q1 |
| Lower D-type flip-flop | Q2 |
| Unlock (this section) | UNLOCK |
| Unlock (next section) | Unlock |

Symbol mapping used for the analysis of the given circuit

Figure 1: Given Circuit



Circuit given to be analyzed

Boolean Equations

UNLOCK = Q1(Q2⊕Q0)

Q2\* = Q2Q0IN'+Q1Q0'

Q1\* = Q2Q1'Q0'IN+Q0IN'

Q0\* = IN

These Boolean equations were generated by analyzing the given circuit, the “And” gate with nots on all inputs and output was analyzed as an or gate due to both having the same functionality.

Through the evaluation of the Boolean equation for UNLOCK, this circuit is understood as a Moore device due to IN not being in the output’s Boolean equation.

Table 2: Simplified state table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  | Input | |  |
| Q2 | Q1 | Q0 | 0 | 1 | Unlock |
| 0 | 0 | 0 | 000 | 001 | 0 |
| 0 | 0 | 1 | 010 | 001 | 0 |
| 0 | 1 | 0 | 100 | 101 | 0 |
| 0 | 1 | 1 | 010 | 001 | 1 |
| 1 | 0 | 0 | 000 | 011 | 0 |
| 1 | 0 | 1 | 110 | 001 | 0 |
| 1 | 1 | 0 | 100 | 101 | 1 |
| 1 | 1 | 1 | x | x | x |

State table created with Boolean equations and later simplifying after noticing 111 is never entered.

Figure 2: State Diagram for given circuit

A picture containing text

Description automatically generated

Made with state table with states relabeled and state diagram simplified.

Codes: 1001, 1010

Timing Information for Figure 1 in ns

pd,io (min) = not applicable, Moore device

pd,io (max) = not applicable, Moore device

setup = 19

hold = 1

pd,co (min) = 8

pd,co (max) = 18

Period = 27

Frequency = 1/(27ns)

**Sequential Circuit Design**

**Moore Device**

Figure 3: Moore State Diagram

Diagram

Description automatically generated

State diagram generated with the requirements needed for the circuit.

Table 3: Moore State Table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  | Input | |  |
| Q2 | Q1 | Q0 | 0 | 1 | Unlock |
| 0 | 0 | 0 | 000 | 001 | 0 |
| 0 | 0 | 1 | 101 | 011 | 0 |
| 0 | 1 | 0 | 000 | 101 | 0 |
| 0 | 1 | 1 | 110 | 011 | 0 |
| 1 | 0 | 0 | 000 | 101 | 1 |
| 1 | 0 | 1 | 100 | 011 | 0 |
| 1 | 1 | 0 | 000 | 111 | 0 |
| 1 | 1 | 1 | 100 | 011 | 1 |

State table generated with the state diagram.

K-Maps for Moore Device

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Unlock |  | Q2 | Q1 |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q0 | 0 | 0 | 0 | 0 | 1 |
|  | 1 | 0 | 0 | 1 | 0 |

Unlock = Q2Q1'Q0'+Q2Q1Q0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q2\* |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 0 | 0 | 0 |
| Q1 | 01 | 0 | 1 | 0 | 1 |
|  | 11 | 0 | 1 | 0 | 1 |
|  | 10 | 0 | 1 | 0 | 1 |

Q2\* = Q1Q0'IN+Q2Q0'IN+Q1QOIN'+Q2Q0IN'

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q1\* |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 0 | 1 | 1 |
| Q1 | 01 | 0 | 0 | 1 | 1 |
|  | 11 | 0 | 1 | 1 | 0 |
|  | 10 | 0 | 0 | 1 | 0 |

Q1\* = Q2'Q0+Q2Q1IN+Q2Q0IN

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q0\* |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 1 | 1 | 0 |
| Q1 | 01 | 0 | 1 | 1 | 0 |
|  | 11 | 0 | 1 | 1 | 0 |
|  | 10 | 0 | 1 | 1 | 0 |

Q0\* = IN

Figure 4: Moore Implication Chart



The chart shows that there are no two pairs of states that can be combined and therefore the current design already contains the minimal number of states.

Figure 5: Moore Device Implemented



Moore device implemented following the Boolean equations generated with K-Maps.

Figure 6: Moore Device Logging



Log of the testing done on the circuit to ensure functionality.

Timing Information for Moore Device in ns

pd,io (min) = not applicable, Moore device

pd,io (max) = not applicable, Moore device

setup = 21

hold = 1

pd,co (min) = 11

pd,co (max) = 20

Period = 29

Frequency = 1/(29ns)

**Mealy Device**

Figure 7: Mealy State Diagram

Diagram, shape

Description automatically generated

State diagram generated with the requirements needed for the circuit.

Table 4: Mealy State Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  | Input | |
| Q2 | Q1 | Q0 | 0 | 1 |
| 0 | 0 | 0 | 000/0 | 001/0 |
| 0 | 0 | 1 | 010/0 | 011/0 |
| 0 | 1 | 0 | 000/0 | 101/0 |
| 0 | 1 | 1 | 110/0 | 011/0 |
| 1 | 0 | 0 | xxx | xxx |
| 1 | 0 | 1 | 010/1 | 011/0 |
| 1 | 1 | 0 | 000/0 | 101/1 |
| 1 | 1 | 1 | xxx | xxx |

State table generated with the state diagram.

K-Maps for Mealy Device

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Unlock |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 0 | 0 | 0 |
| Q1 | 01 | 0 | 0 | 0 | 0 |
|  | 11 | 0 | 1 | x | x |
|  | 10 | x | x | 0 | 1 |

Unlock = Q2Q0'IN+Q2Q0IN'

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q2\* |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 0 | 0 | 0 |
| Q1 | 01 | 0 | 1 | 0 | 1 |
|  | 11 | 0 | 1 | x | x |
|  | 10 | x | x | 0 | 0 |

Q2\* = Q1Q0'IN+Q2Q0IN'

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q1\* |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 0 | 1 | 1 |
| Q1 | 01 | 0 | 0 | 1 | 1 |
|  | 11 | 0 | 0 | x | x |
|  | 10 | x | x | 1 | 1 |

Q1\* = Q0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q0\* |  | Q0 | IN |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 | 00 | 0 | 1 | 1 | 0 |
| Q1 | 01 | 0 | 1 | 1 | 0 |
|  | 11 | 0 | 1 | x | x |
|  | 10 | x | x | 1 | 0 |

Q0\* = IN

Figure 8: Mealy Implication Chart



The chart shows that there are no two pairs of states that can be combined and therefore the current design already contains the minimal number of states.

Figure 9: Mealy Device Implemented



Mealy device implemented following the Boolean equations generated with K-Maps.

Figure 10: Mealy Device Logging



Log of the testing done on the circuit to ensure functionality.

Timing Information for Mealy Device in ns

pd,io (min) = 5

pd,io (max) = 12

setup = 17

hold = 1

pd,co (min) = 11

pd,co (max) = 20

Period = 25

Frequency = 1/(25ns)

**Questions to Answer**

Moore required more hardware. They both required the same amount of memory. Mealy has the more complex timing. Moore would be harder to code break because it requires all 4 inputs to be committed to memory while Mealy only requires 3, this difference doubles the possible codes that need to be tested to break the code. Moore was easier to design.

**Conclusion**

Experience designing and simulating simple sequential logic circuit using flip-flops has been gained.